Abstract of the Disclosure

A synchronous type semiconductor memory device includes a memory cell array in which memory cells are arranged in a matrix; a row address decoder which activates one of word lines in said memory cell array based on a row address in response to a word activation signal; a column decoder which activates one of bit line pairs in said memory cell array based on a column address; and a sense amplifier circuit which amplifies a voltage difference on the activated bit line pair in response to a sense amplifier activation signal. The synchronous type semiconductor memory device further includes a clock data storage section which stores clock data showing a frequency or period of an external clock signal; and a control section which generates the word activation signal based on a row address strobe signal, and generates the sense amplifier activation signal based on the clock data and the row address strobe signal in response to an internal clock signal synchronous with the external clock signal.